Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A memory device comprising:

at least one bank comprised of memory cells organized into a plurality of rows of memory cells; and

control logic coupled to the at least one bank, and responsive to the receipt by the memory device of a single row activate command to open a first row such that if no rows are open when the row activate command is received then the first row within the at least one bank is opened, and that if a different row from the first row in the bank is open when the row activate command is received then the different row is closed and the first row is opened.

2. (Previously Presented) The memory device of claim 1, wherein the memory device is a dynamic random access memory, wherein the row activate command is received via a memory bus coupled to the memory device, and wherein the transfer of data across the memory bus is synchronized to a clock signal transmitted across the memory bus such that portions of data are able to be transferred with each half clock cycle.

3. (Previously Presented) The memory device of claim 1, wherein the control logic is adapted to close the different row only in response to the receipt of an explicit precharge command.

4. (Previously Presented) The memory device of claim 1 in communication with a processor to provide an indication, that is readable by another device, of an ability of the control logic of the memory device to both open the first row and close a different row in response to receipt of the single row activate command to open the first row.

5. (Cancelled).

6. (Cancelled).

7. (Currently Amended) A controlling device comprising:

a ~~memory device including a~~ first storage location in which data concerning rows within a bank of memory cells within ~~the~~ a memory device is stored; and

control logic in communication with the first storage location to check data within the first storage location to determine if a specific row is already open within the bank, to check data within the first storage location to determine if a different row is open if the specific row is not already open, to transmit a row activate command and wait a first predetermined period of time for the row activate command to open the specific row to be carried out if the specific row is determined to not be open and no other rows are open within the bank before transmitting an access command involving that bank, and to transmit a single row activate command that further implies a precharge command and wait a second predetermined period of time for both the row activate command to open the specific row and the implied precharge command as part of the same single row activate command to close the different row to be carried out if the specific row is determined to not be open and a different is open within the bank before transmitting an access command involving that bank.

8. (Original) The controlling device of claim 7, wherein a row activate command is transmitted by the control logic to the memory device via a memory bus coupled to both the controlling device and the memory device, and wherein the transfer of data across the memory bus is synchronized to a clock signal transmitted across the memory bus such that portions of data are able to be transferred with each half clock cycle.

9. (Currently Amended) The controlling device of claim 7, further comprising a second storage location coupled to the control logic to store an indication from a memory device as to whether or not the memory device is capable of responding to the receipt of a single row activate command to open a specific row in a bank where a different row is open by carrying out a precharge operation to close the different row and carrying out a row activate operation to open the specific row.

10. (Original) The controlling device of claim 9, wherein the second storage location further stores an indication from the memory device of the length of the period of time required by the memory device to carry out the precharge operation to close the different row.

11. (Original) The controlling device of claim 9, wherein the control logic accesses the second storage location to check whether or not a given memory device is capable of responding to the receipt of a row activate command to open a specific row in a bank where a different row is open by carrying out a precharge operation to close the different row and carrying out a row activate command to open the specific row.

12. (Currently Amended) A computer system comprising:

a processor;

a memory device having at least one bank in which a plurality of memory cells are organized into rows; and

a memory controller coupled to the processor and to the memory device to transmit a row activate command to open a specific row within the at least one bank of the memory device and wait a first predetermined period of time for a row activate operation to be carried out by the memory device before transmitting a data access command to the specific row if there are no rows open within the at least one bank, and to transmit a single row activate command with an implicit precharge operation to (i) open a specific row within the at least one bank of the memory device and (ii) wait a second predetermined period of time for both thea precharge operation associated with the single row activate command to close a different row and a row activate operation associated with the single row activate command to be carried out before transmitting a data access command to the specific row if a different row other than the specific row is open.

13. (Previously Presented) The computer system of claim 12, wherein the memory controller includes a plurality of buffers includes status information whether the specific row and the different row is open.

14. (Previously Presented) The computer system of claim 13, wherein the plurality of buffers within the memory controller correspond to a number of banks within the memory device.

15. (Original) The computer system of claim 12, wherein the memory controller and the memory device are coupled via a memory bus on which the transfer of data is synchronized to a clock signal transmitted across the bus, and wherein portions of data can be transferred at least on every half clock cycle.

16. (Previously Presented) A method comprising:

determining whether or not a specific row within a bank of memory cells in which a plurality of memory cells are organized into rows within a memory device is open;

determining whether or not a different row within the bank is open if the specific row is closed;

transmitting a first row activate command to the memory device to open the specific row and waiting for a first predetermined period of time for a row activate operation to be carried out by the memory device before transmitting a command for a data access operation involving the specific row to the memory device if it is determined that no rows are open within the bank; and

transmitting a second row activate command to the memory device and waiting for a second predetermined period of time for both a row activate operation to open the specific row and a precharge operation to close a different row to be carried out by the memory device before transmitting a command for a data access operation involving the specific row to the memory device if it is determined that a different row is open within the bank.

17. (Previously Presented) The method of claim 16, wherein determining whether or not the specific row within the bank of memory cells is open includes accessing a specific buffer within a memory controller that transmits the row activate command to open the specific row.

18. (Cancelled).

19. (Currently Amended) A method comprising:

receiving a single row activate command to open a specific row within a bank of memory cells in which a plurality of memory cells are organized into rows;

carrying out a row activate operation in response to the single row activate command to open the specific row if no rows are opened in the bank; and

carrying out both a precharge operation in response to the single row activate command to close a different row and a row activate operation to open the specific row if the specific row is closed and the different row is open.

20. (Previously Presented) The method of claim 19, further comprising providing the memory controller an indication of a memory device having the capability to respond to the transmission of a row activate command to activate a specific row within a bank by carrying out a precharge command to close a different row within the bank in addition to carrying out a row activate command to open the specific row if the specific row is closed and the different row is open.

21. (Currently Amended) A machine-accessible medium comprising code that when executed by a processor within an electronic device, causes the electronic device to:

check whether or not a memory device is capable of responding to a row activate command to open a specific row in a bank of memory cells having a plurality of memory cells organized into rows by carrying out both a precharge operation to close a different row and a row activate operation to open the specific row if the specific row is closed and the different row is open;

program a memory controller to transmit a single row activate command to activate a specific row in a bank when the specific row is closed and a different row is open and to wait a predetermined period of time for the memory device to carry out both a precharge command to close the different row and row activate command to open the specific row before transmitting a data access command involving the specific row to the memory device.

22. (Cancelled).